DATA SHEET

TDA8340
TDA8341
Television IF amplifier and demodulator

Product specification
File under Integrated Circuits, IC02

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Philips Semiconductors

PHILIPS

Television IF amplifier and demodulator

TDA8340
TDA8341

DESCRIPTION

The TDA8340;Q and TDA8341;Q are integrated IF amplifier and demodulator circuits for colour or black/white television receivers, the TDA8340;Q is for application with n-p-n tuners and the TDA8341;Q for p-n-p tuners.

The TDA8340;Q and TDA8341;Q are pin-compatible successors with improved performance to types TDA2540/2541;Q and TDA3540/3541;Q.

Features

- Full range gain-controlled wide-band IF amplifier
- Linear synchronous demodulator with excellent intermodulation performance
- White spot inverter
- Wide-band video amplifier with noise protection
- AFC circuit with AFC on/off switching and sample-and-hold function
- Low impedance AFC output
- AGC circuit with noise gating
- Tuner AGC output for n-p-n tuners (TDA8340) or p-n-p tuners (TDA8341)
- External video switch for switching-off the video output
- Reduced sensitivity for high sound carriers
- Integrated filter to limit second harmonic IF signals
- Wide supply voltage range
- Requires few external components

QUICK REFERENCE DATA

PARAMETER	CONDITIONS	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply voltage (pin 11)		$V_{CC} = V_{11-13}$	9,4	12	13,2	V
Supply current (pin 11)		I_{11}	30	42	55	mA
IF input sensitivity (r.m.s. value)		$V_{1-16(rms)}$	20	40	80	µV
IF gain control range		G_v	–	67	–	dB
Video output voltage (peak-to-peak value)	white signal; 10% top sync	$V_{12-13(p-p)}$	2,4	2,7	3,0	V
Signal-to-noise ratio	V_i = 10 mV	S/(S+N)	50	58	–	dB
AFC output voltage swing (peak-to-peak value)		$V_{5-13(p-p)}$	–	10	–	V

PACKAGE OUTLINES

TDA8340; TDA8341: 16-lead DIL; plastic (SOT38); SOT38-1; 1996 november 29.

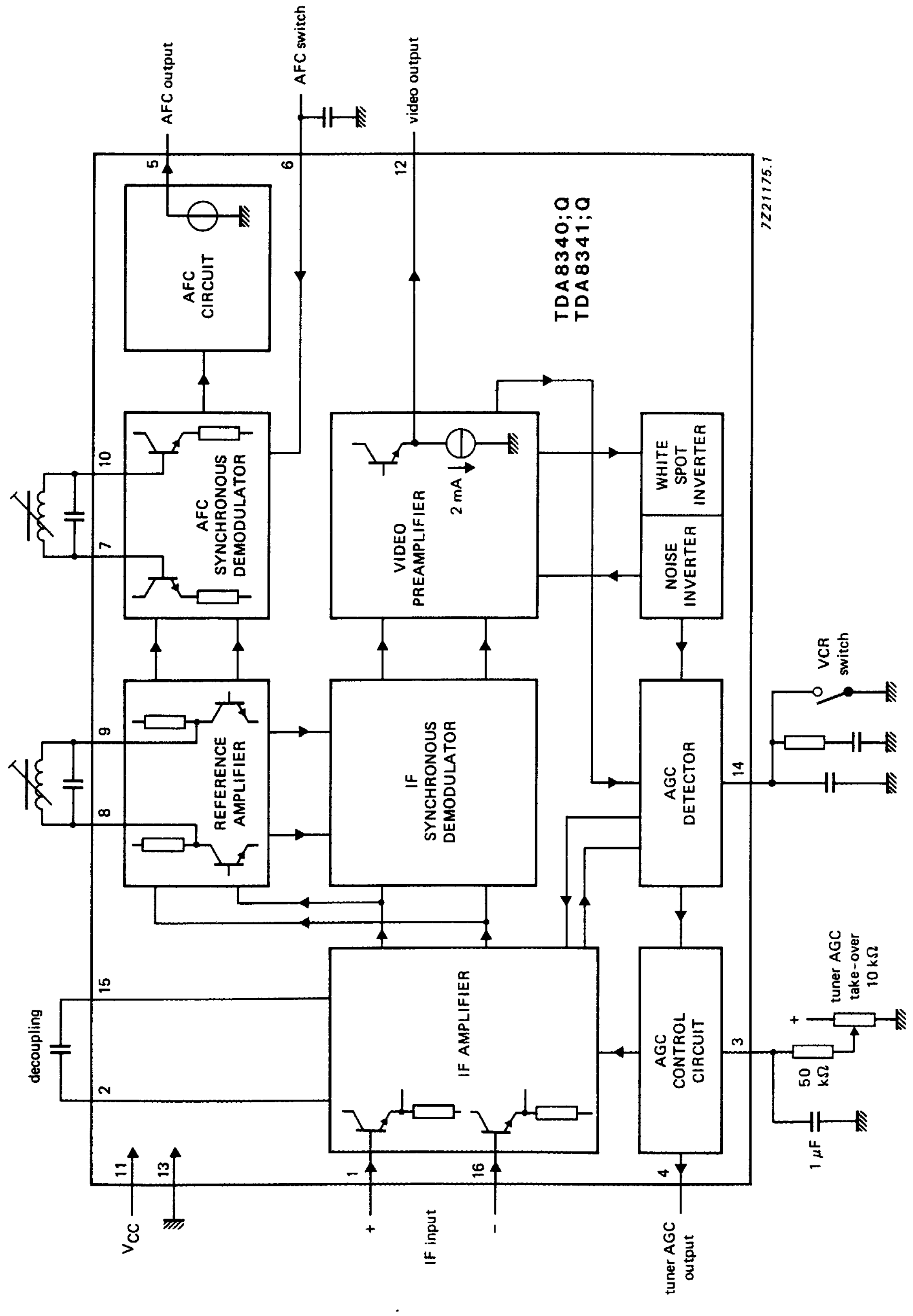


Fig.1 Block diagram.

PINNING

1 and 16	Balanced IF inputs
2 and 15	IF amplifier decoupling
3	Tuner AGC starting point adjustment
4	Tuner AGC output
5	AFC output
6	AFC on/off switch and sample-and-hold capacitor
7 and 10	Reference carrier $\pi/2$ rad. phase shift
8 and 9	IF picture carrier passive regeneration
11	Positive supply voltage (V_{CC})
12	Video output
13	Ground (V_{EE})
14	IF AGC capacitor and VCR switch

FUNCTIONAL DESCRIPTION

IF amplifier

This is a 3-stage, gain-controlled IF amplifier with a wide dynamic range. On-chip capacitors in the d.c. feedback loop of the amplifier maintain stability at maximum gain. Internal stabilization of the supply voltage ensures the desired sensitivity and gain control range over the whole supply voltage range and also gives very good power supply ripple rejection in this part of the circuit.

Demodulator

The redesigned IF demodulator is a quasi-synchronous circuit that employs passive carrier regeneration and logarithmic clamping to give improved signal handling. The demodulator input is a.c. coupled to the IF amplifier to reduce d.c. offsets and thus minimize residual IF carrier in the output signal.

Video amplifier

The linearity and bandwidth of the video amplifier are sufficient to meet all wide band requirements, e.g. for teletext transmissions. Second harmonics of the IF carrier are effectively reduced by a Sallen-Key low pass interstage filter between the demodulator output and the video amplifier input. An integrated filter in the noise inverter reduces the sensitivity of the video amplifier for high sound carriers.

White spot protection comprises a white spot clamp system combined with a delayed-action inverter which is also highly resistant to high sound carriers.

Note. To prevent radiated video output at the input pins, connect a 6,8 µH inductor in series with pin 12 and fit as close as possible to the IC body. Use short leads.

AGC detector

A Bessel low-pass filter between the video output and the AGC detector improves the detector function in the presence of high sound carriers. No ‘hang-up’ occurs in the detector after pin 14 has been short-circuited to ground (VCR switch operated). The detector also generates the sample-and-hold pulse for the AFC system.

AGC control circuit

This converts the AGC detector voltage (pin 14) into a current signal which controls the gain of the IF amplifier. It also provides a tuner AGC control output from pin 4, current limiting is incorporated to prevent internal damage. The AGC starting point is adjusted via pin 3.

AFC circuit

The AFC circuit provides a voltage output which controls the IF frequency of the tuner. Video information on the AFC output (pin 5) is eliminated by a sample-and-hold circuit (external capacitor at pin 6). Coupling between the AFC and reference tuned circuits is via two small capacitors (or parasitic capacitance) between the respective tracks of the printed circuit board. If the capacitance is less than 1 pF, the steepness of the AFC characteristic is reduced.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

PARAMETER	SYMBOL	MIN.	MAX.	UNIT
Supply voltage (pin 11)	$V_{CC} = V_{11–13}$	9,4	13,2	V
IF AGC voltage/VCR switch	$V_{14\text{-}13}$	–	13,2	V
Tuner AGC voltage	$V_{4\text{-}13}$	–	12	V
AFC switch voltage	$V_{6\text{-}13}$	–	13,2	V
Maximum voltage level with VCR switch active	$V_{12\text{-}13}$	–	5,0	V
DC current at video output	I_{12}	–	10	mA
DC current at AFC output	I_5	–	10	mA
Total power dissipation	P_{tot}	–	1,2	W
Storage temperature range	T_{stg}	–55	+150	°C
Operating ambient temperature	T_{amb}	–25	+70	°C

CHARACTERISTICS

Measured in circuit of Fig.3; V_{CC} = 12 V; T_{amb} = 25 °C; unless otherwise specified

PARAMETER	CONDITIONS	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply voltage (pin 11)		$V_{CC} = V_{11-13}$	9,4	12	13,2	V
Supply current	no input signal	I_{11}	30	42	55	mA
IF amplifier (note 1)						
Input sensitivity	at onset of AGC	V_{1-16}	20	40	80	µV
Differential input resistance		R_{1-16}	–	2	–	kΩ
Differential input capacitance		C_{1-16}	–	3	–	pF
Gain control range		G_v	–	67	–	dB
Input signal variation	note 2	V_{12-13}	–	–	0,5	dB
Maximum input signal		V_{1-16}	100	–	–	mV
Tuner AGC (note 1)						
Tuner AGC starting point	R_{3-11} = 39 kΩ	V_{1-16}	–	–	3	mV
(note 3)	R_{3-13} = 39 kΩ	V_{1-16}	70	–	–	mV
Maximum current swing of tuner AGC output		I_4	10	–	–	mA
Input signal variation	note 4; I_4 = 1 to 9 mA	V_{1-16}	–	–	3	dB
Output saturation voltage	I_4 = 7 mA	V_{4-13}	–	200	300	mV
Leakage current	V_4 = 12 V	I_4	–	–	1	µA
Video output (note 4)						
Zero-signal output level	note 5	V_{12-13}	5,7	6,0	6,3	V
Top sync output level		V_{12-13}	2,8	3,0	3,2	V
Video output voltage (peak-to-peak value)	white signal; 10% top sync	$V_{12-13(p-p)}$	2,4	2,7	3,0	V
Internal bias current of emitter follower output transistor			1,4	2,2	3,0	mA
Output impedance		Z_{12}	–	100	–	Ω
Bandwidth of demodulated output signal		B	6	7,5	–	MHz
Differential gain	note 6	G_d	–	2	5	%
Differential phase	note 6	φ_d	–	2	5	deg
Luminance non-linearity	note 7		–	2	5	%
Residual carrier signal (r.m.s. value)	note 8	$V_{12-13(rms)}$	–	2	10	mV

PARAMETER	CONDITIONS	SYMBOL	MIN.	TYP.	MAX.	UNIT
Residual 2nd harmonic of carrier signal (r.m.s. value)	note 8	$V_{12\text{-}13(rms)}$	–	2	10	mV
Variation of video voltage for ΔV_{CC} = 1 V		$\frac{\Delta V_{12-13(p-p)}}{\Delta V_{11-13}}$	0,1	0,2	0,3	
Intermodulation	notes 8 and 9;					
	1,1 MHz, blue	α	–	–65	–60	dB
	1,1 MHz, yellow	α	–	–60	–56	dB
	3,3 MHz	α	–	–	–68	dB
Signal-to-noise ratio	note 10;					
	V_i = 10 mV	S/(S+N)	50	58	–	dB
	max. gain	S/(S+N)	54	61	–	dB
Spot inverter (note 11)						
Threshold level		$V_{12\text{-}13}$	6,3	6,8	7,3	V
Insertion level		$V_{12\text{-}13}$	4,2	4,5	4,8	V
Noise inverter (note 11)						
Threshold level		$V_{12\text{-}13}$	1,6	1,8	2,0	V
Insertion level		$V_{12\text{-}13}$	3,5	3,8	4,1	V
VCR switch						
Level below which video output switches off		$V_{14\text{-}13}$	1,8	2,2	2,6	V
Switch current	V_{12-13} = 0,7 V	$-I_{14}$	40	60	100	µA
AFC circuit (note 12)						
Output voltage swing (peak-to-peak value)		$V_{5\text{-}13(p\text{-}p)}$	–	10	–	V
Change of frequency for an AFC output voltage swing of 10 V		Δf	–	60	120	kHz
AFC output voltage	at f = 38,9 MHz	$V_{5\text{-}13}$	–	6	–	V
	no input signal	$V_{5\text{-}13}$	2	6	10	V
	during AFC off	$V_{5\text{-}13}$	5	6	7	V
AFC output resistance		$R_{5\text{-}13}$	–	500	–	Ω
AFC switch: level below which AFC output switches off		$V_{6\text{-}13}$	1,4	2,0	2,8	V
AFC switch current	during AFC on	I_6	–	200	500	µA
Max. AFC switch current	during AFC off; V_{6-13} = 0 V	I_6	–	–	5	mA

Notes

1. All input signals are measured r.m.s. at top sync and 38,9 MHz.
2. Measured with 0 dB = 200 μV.
3. Tuner AGC starting point is defined as ‘level of input signal when tuner AGC current = 1 mA’.
4. Measured with pin 3 connected via 39 kΩ resistor to V_{CC} (pin 11), with an r.m.s. voltage of 10 mV top sync input signal and with pin 12 not loaded.
5. At the ‘projected zero point’, e.g. with switched demodulator.
6. Measured in the circuit of Fig.7:
   the differential gain is expressed as a percentage of the difference in peak amplitudes between the largest and smallest value relative to the subcarrier amplitude at blanking level;
   the differential phase is defined as ‘the difference (in degrees) between the largest and smallest phase angles’.
7. Measured according to the test line shown in Fig.9:
   the non-linearity is expressed as a percentage of the maximum deviation of a luminance step from the mean step, with respect to the mean step;
   the mean step is (white level – black level) divided by the number of steps.
8. Measured up to 45 dB gain control.
9. Test set-up and input conditions for intermodulation measurements as in Figs 6 and 7.
10. Measured with a 75 Ω source: $S/(S+N) = 20\log\frac{V_{out\ black\ to\ white}}{V_{n(rms)}\ at\ B = 5\ MHz}$
11. Video output waveform showing white spot and noise inverter threshold levels.
12. Measured with input signal $V_{1\text{-}16}$ = 10 mV and with no load at AFC output.

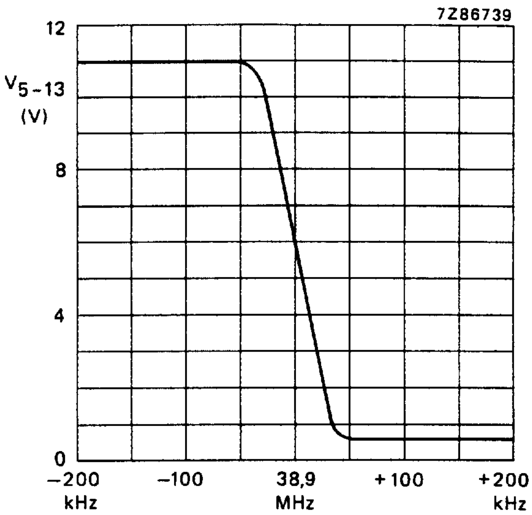


Fig.2 AFC output voltage as a function of frequency.

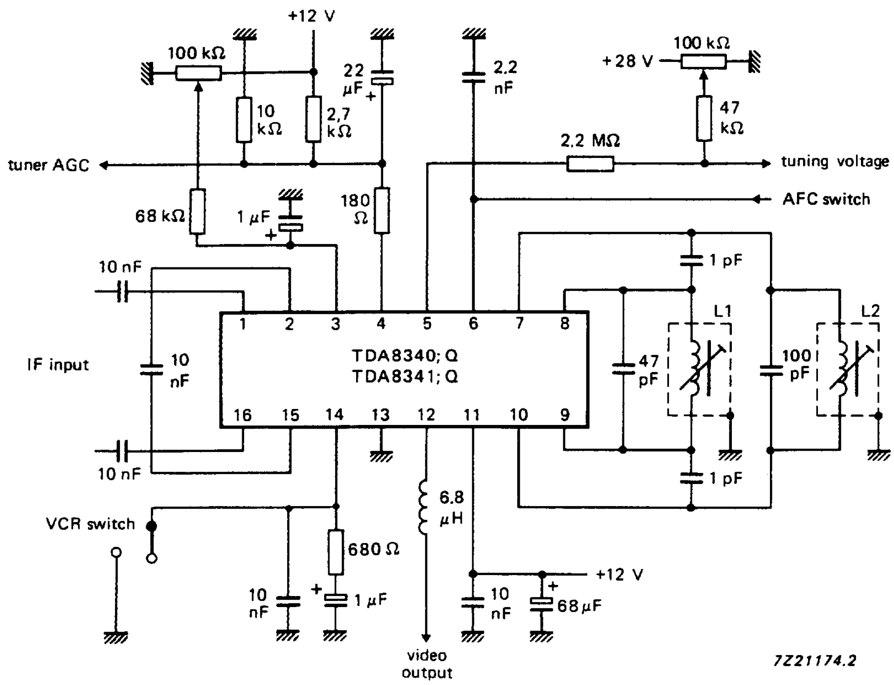


Fig.3 Typical application circuit diagram; Q of L1 and L2 = 80; f_o = 38,9 MHz.

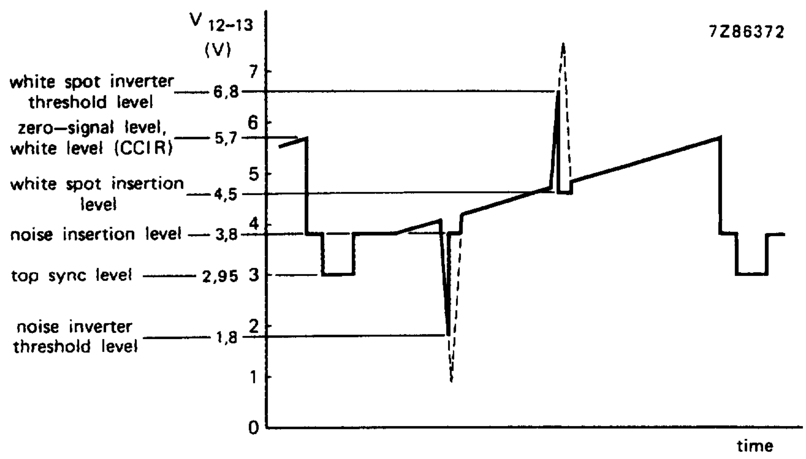


Fig.4 Video output waveform showing white spot and noise inverter threshold levels.

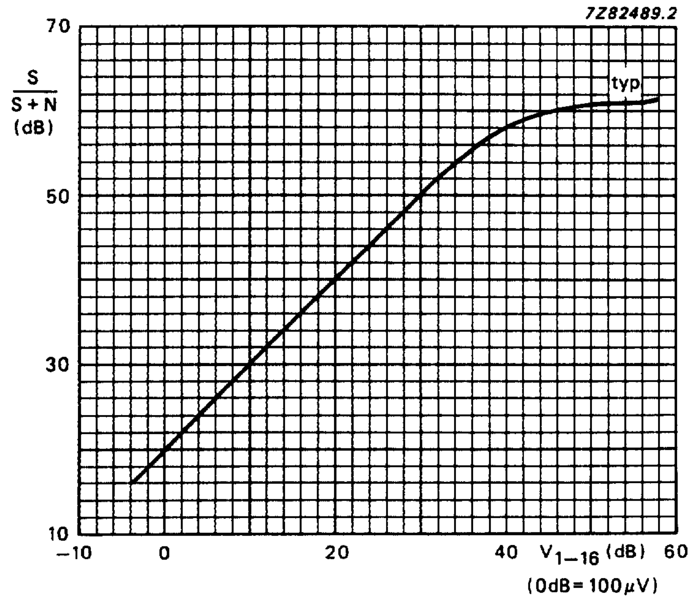
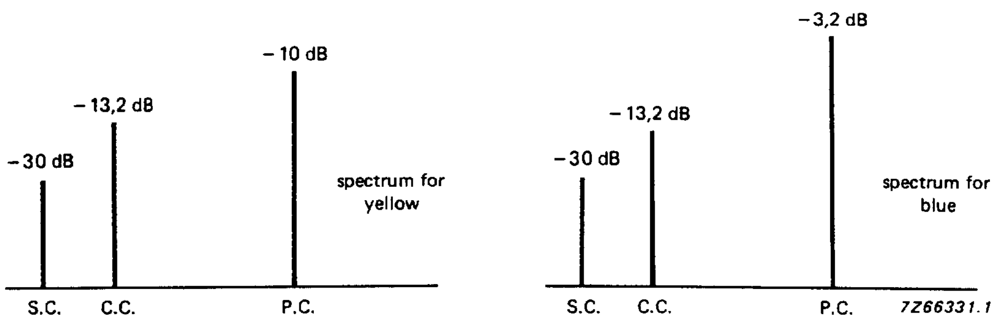


Fig.5 Signal-to-noise ratio as a function of input voltage.



S.C.: sound carrier level ; with respect to top sync level
C.C.: chrominance carrier level ; with respect to top sync level
P.C.: picture carrier level ; with respect to top sync level

Fig.6 Input conditions for intermodulation measurements; standard colour bar with 75% contrast.

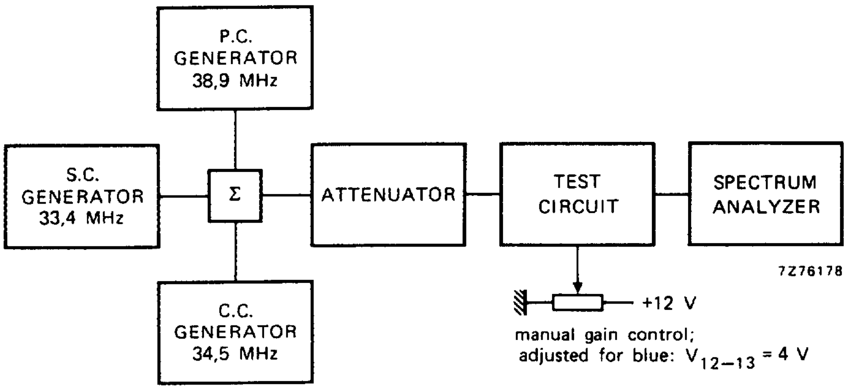


Fig.7 Test set-up for intermodulation measurements.

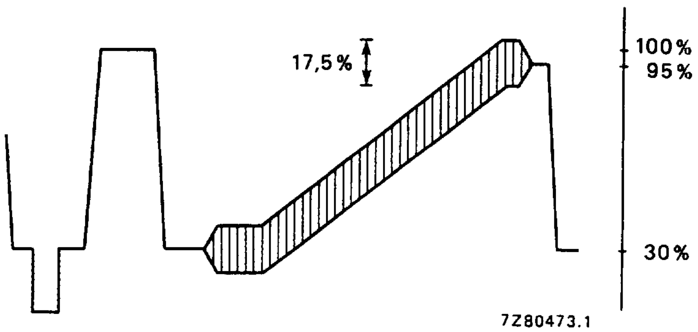


Fig.8 Video output signal.

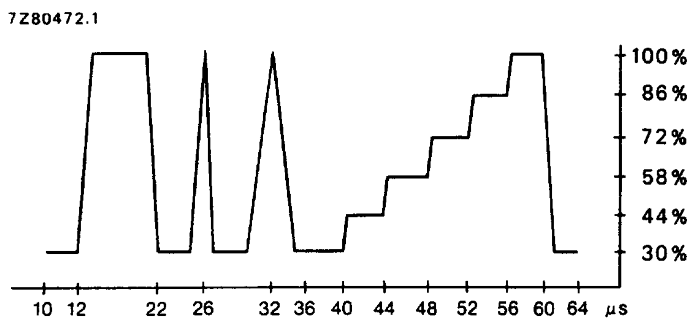
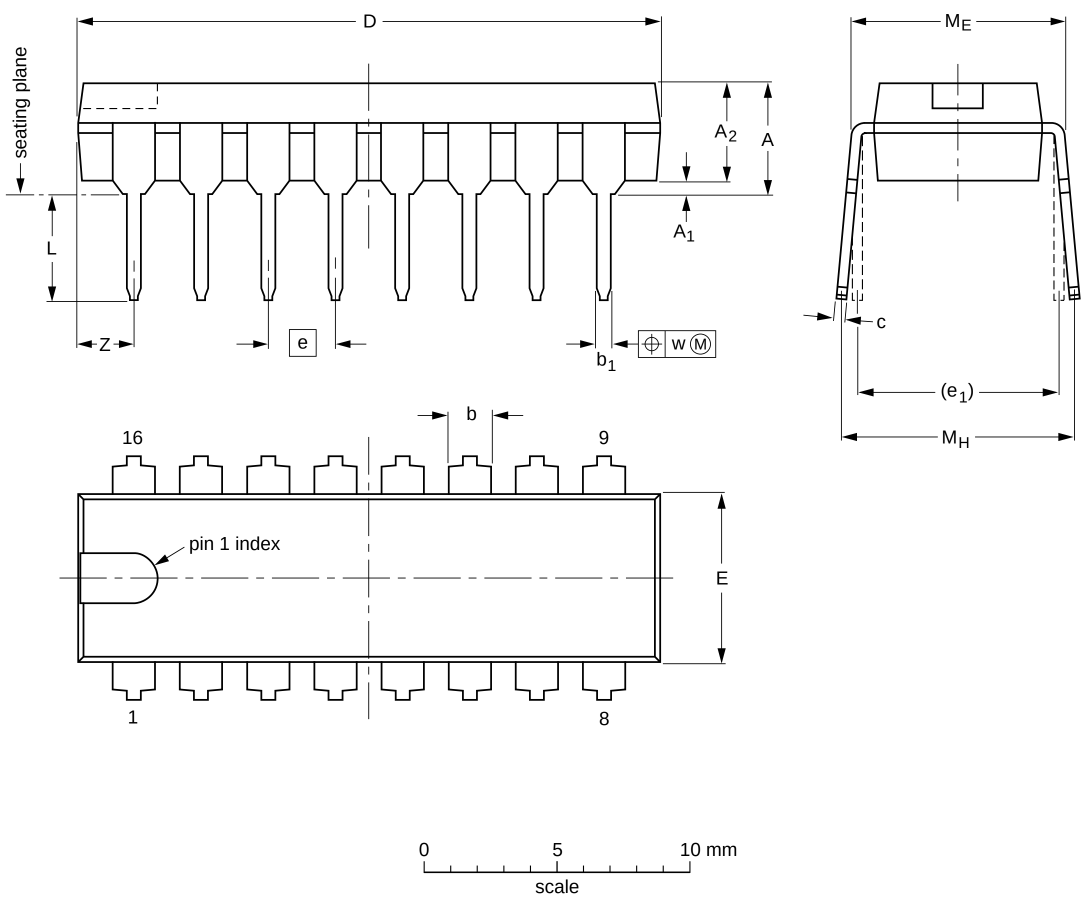


Fig.9 E.B.U. test signal waveform (line 330).

PACKAGE OUTLINE

DIP16: plastic dual in-line package; 16 leads (300 mil); long body **SOT38-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1 min.	A_2 max.	b	b_1	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	4.7	0.51	3.7	1.40 1.14	0.53 0.38	0.32 0.23	21.8 21.4	6.48 6.20	2.54	7.62	3.9 3.4	8.25 7.80	9.5 8.3	0.254	2.2
inches	0.19	0.020	0.15	0.055 0.045	0.021 0.015	0.013 0.009	0.86 0.84	0.26 0.24	0.10	0.30	0.15 0.13	0.32 0.31	0.37 0.33	0.01	0.087

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT38-1	050G09	MO-001AE				~~92-10-02~~ 95-01-19

SOLDERING

Introduction

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *“IC Package Databook”* (order code 9398 652 90011).

Soldering by dipping or by wave

The maximum permissible temperature of the solder is 260 °C; solder at this temperature must not be in contact with the joint for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified maximum storage temperature ($T_{stg\ max}$). If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

Repairing soldered joints

Apply a low voltage soldering iron (less than 24 V) to the lead(s) of the package, below the seating plane or not more than 2 mm above it. If the temperature of the soldering iron bit is less than 300 °C it may remain in contact for up to 10 seconds. If the bit temperature is between 300 and 400 °C, contact may be up to 5 seconds.

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

LIFE SUPPORT APPLICATIONS

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips for any damages resulting from such improper use or sale.